Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

REGULAR EXAMINATION TIMETABLE, JANUARY, 2026
MASTER OF TECHNOLOGY (M. Tech.) All Branches
FIRST YEAR, SEMESTER – I (For 2025 Batch Under Autonomy)
Timings: 10.00 a.m. to 12.00 p.m.

Date: 11th December, 2025

Day & Date	Electronics & Telecommunication Engineering	Computer Engineering
Monday, 19/01/2026	Statistical Signal Processing	Algorithm and Complexity
Wednesday, 21/01/2026	Embedded Systems	Computer Vision
Friday, 23/01/2026	Microstrip Antenna Design	Natural Language Processing
Tuesday, 27/01/2026	Cyber Security and Laws	

Important Note: Changes if any, in the timetable, shall be communicated on the College website (djsce.ac.in).

Ms. Alka Shukla
Controller of Examinations

Dr. Hari Vasudevan
Principal